LISTING OF THE CLAIMS

1. (Previously Presented) A semiconductor integrated circuit device, comprising:

a semiconductor element being formed on a support substrate; and

a heat conduction part formed in an insulation film on the support substrate comprising:

a plurality of metal wiring layers spaced apart from each other and arranged in a vertical stack,

and a plurality of metal via layers connected to the metal wiring layers and coupling the metal wiring layers with each other,

wherein the metal wiring layers are arranged such that they may not transmit a signal to another element of the semiconductor integrated circuit device that is arranged in the same horizontal plane as the heat conduction part.

2. (Original) The semiconductor integrated circuit device as claimed in claim 1, wherein the support substrate comprises one of a semiconductor substrate and a SOI substrate.

3. (Original) The semiconductor integrated circuit device as claimed in claim 1, wherein the heat conduction part comprises an uppermost wiring layer.

4. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 3, further comprising an aperture in the insulation film exposing the uppermost wiring layer.

5. (Original) The semiconductor integrated circuit device as claimed in claim 1, wherein the semiconductor element comprises a MOS transistor and said MOS

transistor comprises one of a fully-depletion type SOI transistor, a partially-depletion type SOI transistor and a SON transistor.

6. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 5, wherein the heat conduction part is directly connected to a gate electrode of the MOS transistor or the heat conduction part is coupled with the gate electrode of the MOS transistor through another element.

7. (Original) The semiconductor integrated circuit device as claimed in claim 5, wherein the heat conduction part is connected to one of a source region and a drain region of the MOS transistor directly or via the connection hole and the metal wiring layer for signal transmission.

8. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 5, further comprising an element separation film arranged to electrically separate the MOS transistor, and wherein the heat conduction part is directly connected to the element separation film or the heat conduction part is coupled with the heat conduction part through another element.

9. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 1, wherein the heat conduction part comprises at least one dummy metal that is not connected to an element of the semiconductor integrated circuit device that is capable of conducting a signal transmission.

10. (Previously Presented) A semiconductor integrated circuit device, comprising:

a plurality of semiconductor elements being formed on a support substrate;

a plurality of function modules being formed by modularizing the plurality of semiconductor elements for each function thereof; and

at least one heat conduction part comprising:

a plurality of metal wiring layers spaced apart from each other and arranged in a vertical stack, and

a plurality of metal via layers connected to the metal wiring layers and coupling the metal wiring layers with each other,

wherein the metal wiring layers are arranged such that they may not transmit a signal to another element of the semiconductor integrated circuit device that is arranged in the same horizontal plane as the heat conduction part, and

wherein at least one of the plurality of function modules comprises one or more of the at least one heat conduction part.

11. (Original) The semiconductor integrated circuit device as claimed in claim 10, wherein the heat conduction part is arranged corresponding to heat capacity of a gate electrode of each of the plurality of function modules.

12. (Original) The semiconductor integrated circuit device as claimed in claim 10, further comprising:

at least one field cell being disposed in an empty space between the function modules, and

wherein one or more of the at least one field cell comprises one or more of the at least one heat conduction part.

13. (Original) The semiconductor integrated circuit device as claimed in claim 12, wherein the field cell having the heat conduction part is disposed corresponding to heat capacity of a gate electrode in a function module.

14. (Withdrawn) A method of fabricating a standard cell type semiconductor integrated circuit device having a plurality of semiconductor elements, the method comprising the steps of:

modularizing the plurality of semiconductor elements for each function thereof so as to form a plurality of function modules;

maintaining the plurality of function modules as standard cells in a library; and

arranging the standard cells in the standard cell type semiconductor integrated circuit device,

wherein at least one of the standard cells comprises a heat conduction part, said heat conduction part comprising the same conductive materials as a connection hole and a metal wiring layer constituting a multi-layer wiring structure, said heat conduction part extending toward an upper layer side along a path different from a wiring path comprising a connection hole and a metal wiring layer for signal transmission.

15. (Withdrawn) The method as claimed in claim 14, wherein the standard cell type semiconductor integrated circuit device comprises at least one field cell being arranged in an empty space between the function modules, said field cell comprising a heat conduction part comprising the same conductive materials as a connection hole and a metal wiring layer constituting a multi-layer wiring structure, said heat conduction part extending toward an upper layer side along a path different from a wiring path comprising a connection hole and a metal wiring layer for signal transmission.

16. (Previously Presented) A semiconductor integrated circuit device, comprising:

a semiconductor element being formed on a support substrate; and

a multi-layer wiring structure being formed in an insulation film on the support substrate, said multi-layer wiring structure comprising:

a signal transmitting part comprising at least one via layer and at least one metal wiring layer to transmit a signal, and

a heat conduction part arranged above the signal transmitting part comprising a first metal layer, a first via layer, and a second metal layer, wherein the the heat conduction part is arranged such that it may not transmit a signal to another element of the semiconductor integrated circuit device that is arranged in the same horizontal plane as the heat conduction part.

17. (Previously Presented) The semiconductor integrated circuit device of claim 16, further comprising:

a second via layer connecting the first metal layer to the at least one metal wiring layer.